In the Claims:

A complete listing of the claims is provided below with proper claim identifiers.

1-20. (Cancelled)

21. (Currently Amended) A high frequency wideband 180° phase switch circuit for insertion into a external circuit having ~~a~~ an input signal port, an output signal port, and a characteristic impedance Z_0, the circuit comprising:

a first input port;

a second input port;

a first output port;

a second output port;

a first waveguide coupled between the first input port and the second input port;

a second waveguide coupled between the first output port and the second output port;

a third waveguide coupled between the first input port and the first output port;

a fourth waveguide coupled between the second input port and the second output port; and

a fifth waveguide coupled between central points of the third waveguide and the fourth waveguide;

where:

at a center frequency of a pre-determined frequency band, each of the waveguides is a half wavelength waveguide with respect to the center frequency;

the first, second, third, and fourth waveguides have a first impedance approximately given by $\sqrt{2}Z_0$; and

the fifth waveguide has a second impedance approximately given by $\frac{Z_0}{\sqrt{2}}$.

22. (Currently Amended) The circuit of claim 21, where at least one of the first and second impedances is a simulation optimized impedance selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at~~

~~least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

23. (Currently Amended) The circuit of claim 21, further comprising at least one of a FET switch, HEMT switch, and PIN diode switch connected in series with at least one of the input and output ports~~, and where the switch comprises at least one of a FET, HEMT, and PIN diode~~.

24. (Previously Presented) The circuit of claim 22, further comprising at least one of a FET switch, HEMT switch, and PIN diode switch connected in series with at least one of the input and output ports.

25. (Currently Amended) The circuit of claim 23, where:

each switch connected to an input port connects to the input signal port ~~no other input port~~; and

each switch connected to an output port connects to the output signal port ~~no other output port~~,

the switches providing switching of the input signal port between the first and second input ports, and the output signal port between the first and second output ports ~~input and output ports~~.

26. (Currently Amended) The circuit of claim 24, where:

each switch connected to an input port connects to the input signal port ~~no other input port~~; and

each switch connected to an output port connects to the output signal port ~~no other output port~~,

the switches providing switching of the input signal port between the first and second input ports, and the output signal port between the first and second output ports. ~~input and output ports~~.

27. (Currently Amended) The circuit of claim 23, where:

each switch connected to an input port connects to ~~that input port~~ the input signal port through a half wavelength, at the center frequency, ~~Z_0 impedance~~ waveguide~~, and connects to no other input port~~; and

each switch connected to an output port connects to ~~that output port~~ the output signal port through a half wavelength, at the center frequency, ~~Z_0 impedance~~ waveguide~~, and connects to no other output port~~,

the switches providing switching of the input signal port between the input ports and output signal port between the output ports.

28. (Currently Amended) The circuit of claim 24, where

each switch connected to an input port connects to ~~that input port~~ the input signal port through a half wavelength, at the center frequency, ~~Z_0 impedance~~ waveguide~~, and connects to no other input port~~; and

each switch connected to an output port connects to ~~that output port~~ the output signal port through a half wavelength, at the center frequency, ~~Z_0 impedance~~ waveguide~~, and connects to no other output port~~,

the switches providing switching of the input signal port between the input ports and output signal port between the output ports.

29. (Currently Amended) The circuit of claim 23, where:

each switch connected to an input port connects to ~~that input port~~ the input signal port through a ~~Z_0 impedance~~ waveguide~~, and connects to no other input port~~;

each switch connected to an output port connects to the output signal port ~~that output port~~ through a ~~Z_0 impedance~~ waveguide~~, and connects to no other output port~~; and

further comprising a series terminating switch, comprising at least one of a FET, HEMT, and a PIN diode switch, connected to each ~~Z_0 impedance~~ waveguide;

the switches providing switching of the input signal port between the input ports and the output signal port between the output ports.

30. (Currently Amended) The circuit of claim 24, where:

each switch connected to an input port connects to ~~that input port~~ the input signal port through a ~~Z_0 impedance~~ waveguide~~, and connects to no other input port~~;

each switch connected to an output port connects to ~~that output port~~ the output signal port through a ~~Z_0 impedance~~ waveguide~~, and connects to no other output port~~; and

further comprising a series terminating switch, comprising at least one of a FET, HEMT, and a PIN diode switch, connected to each ~~Z_0 impedance~~ waveguide;

the switches providing switching of the input signal port between the input ports and the output signal port between the output ports.

31. (Currently Amended) The circuit of claim 21, further comprising:

~~a~~ first parallel switches, ~~connected to~~ each terminating ~~a~~ first quarter wavelength, at the center frequency, ~~Z_0 impedance~~ waveguides connected to at least one of the input ports; and

~~a~~ second parallel switches, ~~connected to~~ each terminating ~~a~~ second quarter wavelength, at the center frequency, ~~Z_0 impedance~~ waveguides connected to at least one of the output ports,

the first and second switches ~~connected in parallel to at least one of the input ports and output ports, and each~~ comprising at least one of a FET, HEMT, and PIN diode.

32. (Currently Amended) The circuit of claim 22, further comprising:

~~a~~ first parallel switches, ~~connected to~~ each terminating ~~a~~ first quarter wavelength, at the center frequency, ~~Z_0 impedance~~ waveguides connected to at least one of the input ports; and

~~a~~ second parallel switches, ~~connected to~~ each terminating ~~a~~ second quarter wavelength, at the center frequency, ~~Z_0 impedance~~ waveguides connected to at least one of the output ports,

the first and second switches ~~connected in parallel to at least one of the input ports and output ports, and each~~ comprising at least one of a FET, HEMT, and PIN diode.

33. (Currently Amended) The circuit of claim 31, where:

~~the~~ each first switch connects to ~~only one of the input and output ports~~ the input signal port through ~~a~~ third quarter wavelength, at the center frequency, ~~Z_0 impedance~~ waveguides;

~~the~~ each second switch connects to ~~only one of the input and output ports~~ the output signal port through ~~a~~ fourth quarter wavelength, at the center frequency, ~~Z_0 impedance~~ waveguides;

the first switches providing switching of the input signal port between the input ports and the second switches providing switching of the output ports to the output signal port.

34. (Currently Amended) The circuit of claim 32, where:

~~the~~ each first switch connects to ~~only one of the input and output ports~~ the input signal port through ~~a~~ third quarter wavelength, at the center frequency, ~~Z_0 impedance~~ waveguides;

~~the~~ each second switch connects to ~~only one of the input and output ports~~ the output signal port through ~~a~~ fourth quarter wavelength, at the center frequency, ~~Z_0 impedance~~ waveguides;

the first switches providing switching of the input signal port between the input ports and the second switches providing switching of the output ports to the output signal port.

35. (Currently Amended) The circuit of claim 23, where at least one of the first and second impedances is a simulation optimized impedance selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of

the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

36. (Currently Amended) The circuit of claim 24, where at least one of the first and second impedances is a simulation optimized impedance selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

37. (Currently Amended) The circuit of claim 25, where at least one of the first and second impedances is a simulation optimized impedance selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

38. (Currently Amended) The circuit of claim 26, where at least one of the first and second impedances is a simulation optimized impedance selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

39. (Currently Amended) The circuit of claim 27, where at least one of the first and second impedances is a simulation optimized impedance selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

40. (Currently Amended) The circuit of claim 28, where at least one of the first and second impedances is a simulation optimized impedance selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

41. (Currently Amended) The circuit of claim 29, where at least one of the first and second impedances is a simulation optimized impedance selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

42. (Currently Amended) The circuit of claim 30, where at least one of the first and second impedances is a simulation optimized impedance selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

43. (Currently Amended) The circuit of claim 31, where at least one of the first and second impedances is a simulation optimized impedance selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

44. (Currently Amended) The circuit of claim 32, where at least one of the first and second impedances is a simulation optimized impedance selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at~~

~~least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

45. (Currently Amended) The circuit of claim 33, where at least one of the first and second impedances is a simulation optimized impedance selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

46. (Currently Amended) The circuit of claim 34, where at least one of the first and second impedances is a simulation optimized impedance selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

47. (Currently Amended) The circuit of claim 25, where at least one of the waveguides is a simulation length-optimized waveguide selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

48. (Currently Amended) The circuit of claim 26, where at least one of the waveguides is a simulation length-optimized waveguide selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

49. (Currently Amended) The circuit of claim 27, where at least one of the waveguides is a simulation length-optimized waveguide selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

50. (Currently Amended) The circuit of claim 28, where at least one of the waveguides is a simulation length-optimized waveguide selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

51. (Currently Amended) The circuit of claim 29, where at least one of the waveguides is a simulation length-optimized waveguide selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

52. (Currently Amended) The circuit of claim 30, where at least one of the waveguides is a simulation length-optimized waveguide selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

53. (Currently Amended) The circuit of claim 31, where at least one of the waveguides is a simulation length-optimized waveguide selected to obtain a 180°

phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

54. (Currently Amended) The circuit of claim 32, where at least one of the waveguides is a simulation length-optimized waveguide selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

55. (Currently Amended) The circuit of claim 33, where at least one of the waveguides is a simulation length-optimized waveguide selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.

56. (Currently Amended) The circuit of claim 34, where at least one of the waveguides is a simulation length-optimized waveguide selected to obtain a 180° phase difference between ~~at least one of the first and second input ports and at least one of~~ the first and second output ports for a given input signal applied to one of the first and second input ports, while improving transmission loss and return loss in the pre-determined frequency band.